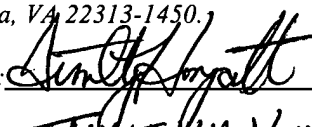TT5516

ASYMMETRIC HALO IMPLANTS

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ASYMMETRIC HALO IMPLANTS

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] This invention relates generally to semiconductor processing, and more particularly to methods of forming halo regions.

2. Description of the Related Art

[0002] A typical field effect transistor implemented on a semiconductor substrate consists of a gate dielectric layer-gate electrode stack positioned on the substrate, and opposing source/drain impurity regions positioned in the substrate below the stack. The lateral separation between the pn junctions of the source/drain regions generally defines the channel length of the transistor. Some source/drain regions include extension regions that project laterally into the channel beneath the gate. When lightly doped, these extension structures are sometime called lightly doped drains ("LDD"). The purpose of the LDD structures is to provide a region of lighter doping beneath the gate electrode to reduce the drain junction potential.

[0003] Scaling of field effect transistor devices has historically been, and continues to be a fundamental goal in the semiconductor fabrication industry. The continual drive toward higher circuit density has been fueled by demands from ordinary consumers, industry, government and the military for ever increasing speed, capability and miniaturization of electronic products, as well as the desire of semiconductor manufacturers to reduce manufacturing costs. Scaling efforts have thus far been highly successful. Two micron processing, considered state of the art a little more than a decade ago, has given way to sub-micron processing.

[0004] As in many aspects of semiconductor processing, current efforts to scale transistor geometry involve a set of trade-offs between higher packing density, improved device performance, and short channel effects. As process technologies scaled below about 2.0 μm, a series of design difficulties arose stemming from the semiconductor physics associated with short-channel devices. Hot carrier effects and punchthrough become much more problematic in short channel devices, such as modern field effect transistors in sub-2.0 μm processing.

Without compensatory processing techniques, short channel effects can either reduce device performance or lead to device failure or both.

[0005] Halo structures have been used for several years in n-channel, p-channel and CMOS technologies as a means of controlling short channel effects in sub-0.5 µm critical dimension processing. A conventional halo structure consists of an implanted impurity region positioned lateral to the LDD of each source/drain region and provided with the same conductivity type as the channel. The conventional method of fabricating a halo structure entails a single large-angle-tilted ("LAT") ion implant that positions the halo structure around and under the vertical junctions of both the LDD and the overlapping heavier doped portion of the source/drain region. Halo regions are formed on both the source side and the drain side of the channel.

[0006] A difficulty associated with conventionally produced halo structures is the potential for limitations on carrier mobility and drive current to exist for a given level of leakage current. Halo regions positioned proximate both the source side and the drain side present an impediment to carrier mobility. The ability to reduce barriers to carrier mobility without significant increases in leakage currents holds the promise of squeezing even more performance out of halo implanted transistors.

[0007] The present invention is directed to overcoming or reducing the effects of one or more of the foregoing disadvantages.

SUMMARY OF THE INVENTION

[0008] In accordance with one aspect of the present invention, a method of manufacturing is provided that includes forming a symmetric transistor and an asymmetric transistor on a substrate. The symmetric transistor has a first gate on the substrate, and a first source/drain region and second source/drain region in the substrate. The asymmetric transistor has a second gate on the substrate, and a first source region and a first drain region in the substrate. A first mask is formed on the substrate with a first opening to enable implantation formation of first and second halo regions proximate the first and second source/drain regions of the symmetric transistor. The first and second halo regions of a first dosage are formed beneath the first gate by implanting off-axis through the first opening at a first twist angle and then a second and substantially opposite twist angle. The first mask is removed and a second mask is formed on the substrate with a second opening to enable implantation formation of a third

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halo region proximate the first source region of the second asymmetric transistor but prevent formation of a halo region proximate the first drain region. The third halo region of a second dosage greater than the first dosage is formed by implanting off-axis through the second opening.

5   [0009] In accordance with another aspect of the present invention, a method of manufacturing is provided that includes forming a symmetric transistor that has a first gate on a substrate, and a first source/drain region and second source/drain region in the substrate. An asymmetric transistor formed that has a second gate on the substrate, and a first source region and a first drain region in the substrate. A first mask is formed on the substrate. The

10   first mask has a first opening that exposes a first portion of the first source/drain region proximate the first gate and a second portion of the second source/drain region proximate the first gate. First and second halo regions of a first dosage are formed beneath the first gate by implanting off-axis through the first opening at a first twist angle and then a second and substantially opposite twist angle. The first mask and the first gate shadow opposite portions

15   of the substrate lateral to the first gate so that the first halo region forms beneath the first gate proximate the first portion of the first source/drain region and the second halo region forms beneath the first gate proximate the second portion of the second source/drain region. The first mask is removed and a second mask is formed on the substrate. The second mask has a second opening that exposes a first portion of the first source region proximate the second

20   gate. A third halo region of a second dosage greater than the first dosage is formed proximate the first portion of the first source region by implanting off-axis through the second opening. The second mask and the second gate shadow portions of the substrate lateral to the second gate so that the first halo region forms beneath the first gate proximate the first portion of the first source region, but no halo region forms proximate the first drain

25   region.

[0010] In accordance with another aspect of the present invention, a method of manufacturing is provided that includes forming a symmetric transistor that has a first gate on a substrate, and a first source/drain region and a second source/drain region in the substrate. A first asymmetric transistor is formed that has a second gate on the substrate, a first source

30   region and a first drain region in the substrate. A second asymmetric transistor is formed that has a third gate on the substrate, a second source region adjacent to the first source region

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and a second drain region. A first mask is formed on the substrate. The first mask has a first opening that exposes a first portion of the first source/drain region proximate the first gate and a second portion of the second source/drain region proximate the first gate. First and second halo regions of a first dosage are formed beneath the first gate by implanting off-axis

5   through the first opening at a first twist angle and then a second and substantially opposite twist angle. The first mask and the first gate shadow opposite portions of the substrate lateral to the first gate so that the first halo region forms beneath the first gate proximate the first portion of the first source/drain region and the second halo region forms beneath the first gate proximate the second portion of the second source/drain region. The first mask is removed

10   and a second mask is formed on the substrate. The second mask has a second opening that exposes a first portion of the first source region proximate the second gate. A third halo region of a second dosage greater than the first dosage is formed proximate the first portion of the first source region by implanting off-axis at a third twist angle through the second opening. The second mask and the second gate shadow portions of the substrate lateral to the

15   second gate so that the first halo region forms beneath the first gate proximate the first portion of the first source region, but no halo region forms proximate the first drain region. The second mask is removed and a third mask is formed on the substrate. The third mask has a third opening that exposes a first portion of the second source region proximate the third gate. A fourth halo region of a third dosage greater than the first dosage is formed proximate

20   the first portion of the second source region by implanting off-axis at a fourth twist angle substantially to the third twist angle through the second opening, the third mask and the third gate shadow portions of the substrate lateral to the third gate so that the fourth halo region forms beneath the third gate proximate the first portion of the second source region, but no halo regions form proximate the first and second drain regions.

25   **BRIEF DESCRIPTION OF THE DRAWINGS**

[0011]   The foregoing and other advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings in which:

[0012]   FIG. 1 is a plan view of a small portion of an integrated circuit in accordance with the present invention;

30   [0013]   FIG. 2 is a cross-sectional view of FIG. 1 taken at section 2-2 in accordance with the present invention;

[0014] FIG. 3 is another plan view of the integrated depicted in FIG. 1 in accordance with the present invention;

[0015] FIG. 4 is a plan view of the integrated circuit depicted in FIG. 3 with a mask formed thereon in accordance with the present invention;

[0016] FIG. 5 is a cross-sectional view of FIG. 4 taken at section 5-5 and depicts halo implantation of a portion of the integrated circuit in accordance with the present invention;

[0017] FIG. 6 is another plan view of the integrated depicted in FIG. 1 in accordance with the present invention;

[0018] FIG. 7 is a plan view of the integrated circuit depicted in FIG. 6 with another mask formed thereon in accordance with the present invention;

[0019] FIG. 8 is a cross-sectional view of FIG. 7 taken at section 8-8 and depicts halo implantation of another portion of the integrated circuit in accordance with the present invention;

[0020] FIG. 9 is another plan view of the integrated depicted in FIG. 1 in accordance with the present invention;

[0021] FIG. 10 is a plan view of the integrated circuit depicted in FIG. 9 with another mask formed thereon in accordance with the present invention; and

[0022] FIG. 11 is a cross-sectional view of FIG. 10 taken at section 11-11 and depicts halo implantation of another portion of the integrated circuit in accordance with the present invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0023] In the drawings described below, reference numerals are generally repeated where identical elements appear in more than one figure. Turning now to the drawings, and in particular to FIG. 1, therein is shown a plan view of a small portion of an integrated circuit 10. The integrated circuit 10 may include many circuit structures, such as resistors, transistors, capacitors and interconnects, to name just a few. A few of the possible circuit structures are depicted in FIG. 1, namely transistor devices 12, 14, 16, 18 and 20. The transistor devices 12, 14, 16, 18 and 20 consist of respective gate structures 22, 24, 26, 28 and 30 positioned over a shared active region 32 that is circumscribed by an isolation structure 34.

[0024] The gate structures 22, 24, 26, 28 and 30 may be fabricated by initially depositing a conducting or semiconducting material layer. The material layer may be composed of a variety of materials, such as, for example, polysilicon, amorphous silicon, aluminum, copper, gold, tantalum or the like. In an exemplary embodiment, the material is polysilicon. Well-known techniques for applying polysilicon, such as chemical vapor deposition ("CVD"), may be used to deposit the material layer. In an exemplary embodiment, the polysilicon is deposited by CVD at or above about 625 °C to a thickness of about 75.0 to 180.0 nanometers. Later impurity implants for source\drain regions to be described below will render the polysilicon conductive.

[0025] The active region 32 is part of a much larger substrate and may be composed of a variety of semiconducting materials, such as, for example, silicon, germanium, or the like. While a shared active region 32 is depicted, it should be understood that the transistor devices 12, 14, 16, 18 and 20 may be alternatively implemented on discrete active regions or a combination of shared and discrete active regions.

[0026] The isolation structure 34 is designed to provide lateral electrical isolation from other electrical structures on the integrated circuit 10. Various structural forms and electrically insulating materials may be used to fabricate the isolation structure 34, such as, for example, shallow trench isolation, deep trench isolation, field oxide, or other isolation structures composed of silicon dioxide, tetra-ethyl-ortho-silicate ("TEOS"), or other suitable isolation materials.

[0027] Vertical electrical isolation for the active region 32 may be provided by impurity wells, by implementing the active region on a semiconductor-on-insulator substrate or other well-known techniques.

[0028] In the illustrated embodiment, the transistor devices 12, 14, 16, 18 and 20 are implemented as field effect transistors. The transistor devices 12, 16, 18 and 20 are implemented as "asymmetric transistors" and the transistor device 14 is implemented as a "symmetric transistor." In an asymmetric transistor, the source and drain do not swap functions during device operation. In a symmetric transistor by contrast, the source and drain do swap functions. Depending upon the interconnections to power, ground or other conductors and the bias state of the symmetric transistor, the portions of the active region on either side of the gate may function as either a source or a drain. This swapping of source

and drain functions is useful in a variety of contexts in integrated circuits, such as, for example, as pass transistors in memory devices. The sources for each of the asymmetric transistors 12, 16, 18 and 20 are labeled "S". The drains for those transistors are labeled "D". The function swapping source/drains for the symmetric transistor 14 are labeled "S/D".

5   [0029]   The sources S, drains D and source/drains S/D may be formed using a variety of well-known techniques for forming source/drain regions such as, for example, ion implantation, diffusion, in-situ doping or the like.

[0030]   The integrated circuit 10 is depicted in FIG. 1 at an intermediary stage of processing that occurs prior to the formation of contacts to the various sources S, drains D and

10   source/drains S/D in the active region 32. The anticipated locations of the later-formed contacts are illustrated by the dashed boxes in the active region 32. Some of the contacts such as the contacts 36, 54, 42 and 48 may be connected to power and are additionally designated V_{cc}.

[0031]   As noted above in the Background section, halo implants have been used as a means

15   of altering the threshold voltage of a field effect transistor. The benefits of utilizing halo regions may be extended by tailoring the implant and masking scheme in order to account for differences between symmetric and asymmetric transistor devices. A goal of the process of the present invention may be understood by referring now also to FIG. 2, which is a cross-sectional view of FIG. 1 taken at section 2-2. The asymmetric device 12 and the symmetric

20   device 14 are visible in FIG. 2, as well as the active region 32 and a small portion of isolation structure 34. At this stage, the gates 22 and 24 of the devices 12 and 14 may have a lateral dimension 2.0λ where λ is some targeted final lateral dimension. For example, the dimension 2.0λ may represent the width of the gates 22 and 24 following lithographic and etch patterning, while the dimension λ may represent the width of the gates 22 and 24 following

25   one or more trim processes, such etch trims. The gates of the other devices 16, 18 and 20, which are not visible in FIG. 2, may have the same lateral dimension as the gates 22 and 24.

[0032]   The device 12 includes a source S and shares an impurity region with the device 14. The portion of the shared impurity region proximate the gate 22 of the asymmetric device 12 is implemented as a drain D but the portion proximate the gate 24 for the symmetric device

30   14 is implemented as a source/drain S/D as described above. The device 14 additionally has a shared impurity region, only a portion of which is visible, which is also implemented as a

source/drain S/D. As described in more detail below, a masking and implant scheme is presented that provides for: (1) the formation of a halo region 55 with a nominal impurity dosage proximate the source S of the asymmetric transistor 12; (2) no formation of a halo region proximate the drain D of the asymmetric device; and (3) and the formation of halo

5   regions 56 and 58 with nominal dosages that are smaller than the impurity region 55 and positions respectively proximate the source/drains S/D of the symmetric transistor 14. For example, the halo region 55 may be established with a nominal dosage 2.0X and the halo regions may be established with a smaller dosage X. The other asymmetric devices 16, 18 and 20 may be advantageously provided with asymmetric halo regions similar to the device

10   12 as depicted in FIG. 2.

[0033] An exemplary process flow for implementing the selective halo formation in accordance with the present invention may be understood by referring now to FIGS. 3, 4, 5, 6, 7, 8, 9, 10 and 11 and initially to FIG. 3. Like FIG. 1, FIG. 3 is a plan view of the integrated circuit 10. Assume for the purposes of illustration that it is desired to first perform

15   halo implants for the symmetric device 14. The portion of the active region 32 targeted for halo implantation is illustrated by the dashed box 60. The dimensions of the target area 60 should be such that a later-formed mask with an opening corresponding to the layout of the target area 60 will shadow the drains D of the devices 12 and 16 during halo implantation to form halo regions 56 and 58 (see FIG. 2) beneath the gate 24. The actual dimensions of the

20   target area 60 will depend on, *inter alia*, the height of the subsequently-formed mask, the dimension λ, and some rules of thumb that are intended to account for potential errors in mask lithography. For example, the target area 60 may be dimensioned so that it: (1) extends laterally a distance of about 5.5λ to either side of the edges of the gate 24; (2) overlaps the isolation structure 34 by about 2.5λ; and (3) is spaced about 1.5λ from the opposing edges of

25   the gates 22 and 26.

[0034] FIG. 4 illustrates a plan view of a masking of the integrated circuit 10 that is a prelude to a halo implantation of the symmetric device 14. A mask 62 is patterned over the integrated circuit 10 with an opening 64 corresponding to the layout of the dashed box 60 in FIG. 3. The opening 64 may have a width W and a length L. Using the aforementioned rules

30   of thumb, the width W may be about 13.0λ and the length L may be about 5.0λ plus the length of the active region 32. The mask 62 may be formed from positive or negative tone

photoresist. The type of photoresist selected will depend on the wavelength of exposure radiation and ability of the resist to be applied with a desire thickness range. In an exemplary embodiment, a JSR Corp.'s KrF M20G positive tone photoresist may be used. Optionally, a hard mask of oxide, nitride, laminates of these or the like may be formed, albeit with a

5   greater process complexity.

[0035]   The opening 64 exposes portions of the underlying symmetric device 14. Note that portions of the active region 32, the isolation structure 34 and the gate 24 are visible. Again, the anticipated positions of the later-formed contacts 34, 40, 52 and 50 are depicted as well. It is desired to halo implant the active region 32 on both sides of and with substantial

10   penetration beneath the gate 24. In this regard, "off-axis" implantation, that is, a tilted-angle implantation at an implant angle θ relative to vertical is used. Since halos are needed for both sides of the gate 24, the halo implants may be performed with a twist, that is, an angle relative to the long axis of the gate 24. The twist angle is usually orthogonal to the long axis of the gate 24 so that greatest penetration beneath the gate 24 is achieved. However, the twist

15   angle may be somewhat less than strictly perpendicular if desired. For the orientation of the gate 24 in FIG. 4, implants will be performed at a "RIGHT" and "LEFT" twist. If desired, halo implants may be performed at four different twists, such as "RIGHT," "LEFT," "TOP," and "BOTTOM" so that other devices on the integrated circuit that are, for example, perpendicular to the orientation of the symmetric device 14, will receive the symmetric halo

20   implants as well. Note that the assignment of directions "RIGHT," "LEFT" etc. to the twist parameters in FIG. 4 is somewhat arbitrary.

[0036]   FIG. 5 depicts a cross-sectional view of FIG. 4 taken at section 5-5. The mask 62 is advantageously formed with a height H_1. The height H_1 is selected in conjunction with the width W of the opening 64 as described above so that the two (or optionally four) halo

25   implants, one with a RIGHT twist and one with a LEFT twist and performed at an implant angle θ with respect to vertical, may establish symmetric X dosage halo regions 56 and 58 beneath the gate 24 as shown. The width W and the height H_1 are selected such that the portions 66 and 68 on either side of the gate 24 are effectively shadowed by the combination of the mask 62 and the gate 24 during implantation. In this way, halos will not be formed

30   proximate the drains D of the asymmetric devices 12 and 16. In an exemplary embodiment, the height H_1 may be about 100.0 to 500.0 nm.

[0037] The parameters for the halo implants are largely matters of design discretion. In an exemplary embodiment, the species may be boron or BF_2 for a n-channel device and arsenic or antimony for a p-channel device. The energy may be about 3 to 80 keV, the nominal dosage X may be about 1E13 to 1E14 cm^{-2} and the angle θ may be about 16 to 45°.

[0038] Following the implantation, the mask 62 is stripped. Stripping may be accomplished by ashing, solvent stripping, combinations of the two or the like.

[0039] With the halo regions 56 and 58 formed for the symmetric device 14, attention is now turned to the formation of the halo regions for the asymmetric devices 12, 16, 18 and 20. As depicted in FIGS. 6-11, this entails two masking steps. Bearing in mind the goal of providing source regions S with 2.0X dosage halos, two separate masking and implantation steps are provided, one each for BOTTOM and LEFT twists and one each for TOP and RIGHT twists. As noted elsewhere herein, the BOTTOM and TOP twists are optional. FIG. 6 depicts a plan view like FIG. 3 of the integrated circuit 10 showing the targeted areas for halo implantation at BOTTOM and LEFT twists. The regions targeted for implantation are illustrated by the dashed boxes 70 and 72. As with the masking for the symmetric implant depicted in FIGS. 3 and 4, the ultimate masking to provide open areas corresponding to the target regions 70 and 72 may be made with a few rules of thumb to guide the selection of dimensions for those regions 70 and 72. As shown, the region 70 may be formed so that it has a lateral dimension that overlaps to one side of the gate 22 of the device 12 by a distance 5.5 λ and on the other side to a distance of 0.5 λ. The overlap to either side of the active region 32 may be about 2.5 λ. The lateral dimension of the targeted region 72 may be selected so that there is a 0.5 λ overlap on one side of the gate 26 of the device 16 and the same 0.5 λ overlap on the opposite side of the gate 30 of the device 20 as shown. Again, the overlaps with the active region 32 may be about 2.5 λ.

[0040] A masking and implantation process corresponding to the desired targeted areas 70 and 72 is illustrated in FIGS. 7 and 8. FIG. 7 is a plan view of the integrated circuit 10 with a mask 74 formed thereon with openings 76 and 78 defined therein and FIG. 8 is a cross-sectional view of FIG. 7 taken at section 8-8. The mask 74 may be formed as described elsewhere herein. The opening 76 corresponds to the targeted region 70 and the opening 78 corresponds to the targeted region 72 shown in FIG. 6. Note that the openings 76 and 78 reveal portions of the underlying transistor devices 12, 16, 18 and 20 as well as the active

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region 32 and the isolation structure 34. As shown in FIG. 8, the mask 74 may be formed with a height, H_2. The H_2 and the length and width of the openings 76 and 78, as illustrated by the dimensions of the targeted regions 70 and 72 in FIG. 6, are selected so that when a halo implant at a LEFT twist is performed as represented by the arrows 80, halo regions 82, 84 and 86 will be formed while the halo regions 56 and 58 of the transistor 14 are shadowed by the combination of the gate 24 and the mask 74. In this way, the size or dosage of existing halo regions 56 and 58 will be unaffected. The parameters for the halo implant may be as generally described elsewhere herein. However, the dosage is selected to be greater than the nominal dosage X for the halo regions 56 and 58 described elsewhere herein. In an exemplary embodiment, the dosage is about 2.0X. Note that if a BOTTOM twist implant is also performed, dosage 2.0X halo regions will be formed in other asymmetric devices orthogonal to the devices depicted in FIG. 8 but not otherwise shown here. Following the implantation, the mask 74 is stripped using ashing, solvent stripping a combination of these or the like.

[0041] With the halo regions 56 and 58 formed for the symmetric device 14, attention is now turned to the second masking and implantation step to perform a RIGHT (and optional TOP) twist implant in order to form a halo region for the source S of the asymmetric device 16. Referring now to FIG. 9, the regions targeted for implantation are illustrated by the dashed boxes 88 and 90. Note that the target region 88 is not truly necessary, and indeed may be eliminated, since the source region S for the device 12 has already been implanted and will be shadowed by the gate 22 during the subsequent RIGHT twist implant. As with the masking for the symmetric implant depicted in FIGS. 3 and 4, the ultimate masking to provide open areas corresponding to the target regions 88 and 90 may be made with a few rules of thumb to guide the selection of dimensions for those regions 88 and 90. As shown, the region 88 may be formed so that it has a lateral dimension that overlaps to one side of the gate 22 of the device 12 by a distance 5.5 λ and on the other side to a distance of 0.5 λ. The overlap to either side of the active region 32 may be about 2.5 λ. The lateral dimension of the targeted region 90 may be selected so that there is a 0.5 λ overlap on one side of the gate 26 of the device 16 and the same 0.5 λ overlap on the opposite side of the gate 28 of the device 18 as shown. Again, the overlaps with the active region 32 may be about 2.5 λ.

[0042] A masking and implantation process corresponding to the desired targeted areas 88 and 90 is illustrated in FIGS. 10 and 11. FIG. 10 is a plan view of the integrated circuit 10 with a mask 92 formed thereon with openings 94 and 96 defined therein and FIG. 11 is a cross-sectional view of FIG. 10 taken at section 11-11. The mask 92 may be formed as

5 described elsewhere herein. The opening 94 corresponds to the targeted region 88 and the opening 96 corresponds to the targeted region 90 shown in FIG. 9. Note that the openings 94 and 96 reveal portions of the underlying transistor devices 12, 16, and 18 as well as the active region 32 and the isolation structure 34. As shown in FIG. 11, the mask 92 may be formed with a height, H_3. The height H_3 and the length and width of the openings 94 and 96,

10 as illustrated by the dimensions of the targeted regions 88 and 90 in FIG. 9, are selected so that when a halo implant at a RIGHT twist is performed as represented by the arrows 98, a halo region 100 will be formed while the halo regions 56 and 58 of the transistor 14 are shadowed. In this way, the size or dosage of existing halo regions 56 and 58 will be unaffected. The halo regions 84 and 86 will be similarly unaffected due to shadowing.

15 [0043] The parameters for the halo implant may be as generally described elsewhere herein. However, the dosage of the halo implant is selected to be greater than the nominal dosage X for the halo regions 56 and 58 described elsewhere herein. In an exemplary embodiment, the dosage is about 2.0X. The energy, implant angle and species may be as described elsewhere herein. Note that if a TOP twist implant is also performed, dosage 2.0X

20 halo regions will be formed in other asymmetric devices orthogonal to the devices depicted in FIG. 10 but not otherwise shown here. Following the implantation, the mask 92 is stripped using ashing, solvent stripping a combination of these or the like.

[0044] While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have

25 been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.